4. A data entry and display control circuit as claimed in claim 1, wherein said microprocessor is operative in response to a predetermined pair of character signals to move the cursor to a predetermined location.

5. A data entry and display control circuit as claimed in claim 1, wherein said microprocessor is operative in response to a predetermined pair of character signals to move the cursor to a predetermined line.

6. A data entry and display control circuit as claimed in claim 1, wherein there is further included:

first sensible indicating means connected to said microprocessor, said microprocessor being operative in response to said first appearance of said switch signal to provide a first sensible control signal, said first sensible indicating means being operative in response to said first sensible control signal to provide a first sensible signal.

7. A data entry and display control circuit as claimed in claim 1, wherein there is further included:

second sensible indicating means connected to said microprocessor, said microprocessor being operative in response to said first appearance of said switch signal to provide a second sensible control signal, said second sensible indicating means being operative in response to said second sensible control signal to provide a second sensible signal.

8. A data entry and display control circuit as claimed in claim 6, wherein said first sensible indicating means comprises a visual signaling means operative in response to said first sensible control signal to provide a first visual signal.

9. A data entry and display control circuit as claimed in claim 7, wherein said second sensible indicating means comprises audible signaling means operative in response to said second control signal to provide a first audible signal.

10. A data entry and display control circuit as claimed in claim 8, wherein said visual signaling means comprises a light emitting diode operative in response to said first sensible control signal to turn on and thereby provide a light signal.

11. A data entry and display control circuit as claimed in claim 9, wherein said second sensible control signal has a predetermined duration; said audible signaling means comprising an audible transducer operative in response to said second sensible control signal to provide a tone of predetermined duration.

12. A data entry and display control circuit as claimed in claim 6, wherein said microprocessor is further operative in response to termination of said first appearance of said switch signal to provide a third sensible control signal, said first sensible indicating means being operative in response to said third sensible control signal to provide a third sensible signal.

13. A data entry and display control circuit as claimed in claim 12, wherein said first sensible indicating means comprising visual signaling means operative in response to said third sensible control signal to provide a second visual signal.

14. A data entry and display control circuit as claimed in claim 13, wherein said visual indicating means comprises a light emitting diode; and said third sensible control signal is a periodic sensible control signal; said light emitting diode being operative in response to said periodic sensible control signal to periodically turn on and off and thereby provide a flashing light signal.

15. A data entry and display control circuit as claimed in claim 6, wherein said microprocessor is further operative in response to said second appearance of said switch signal to provide a fourth sensible control signal, said first sensible indicating means operative in response to said fourth sensible control signal to provide a fourth sensible signal.

16. A data entry and display control circuit as claimed in claim 15, wherein said first sensible indicating means comprises visual signaling means operative in response to said fourth sensible control signal to provide a third visual signal.

17. A data entry and display control circuit as claimed in claim 16, wherein said visual signaling means comprises a light emitting diode operative in response to said fourth sensible control signal to turn off and inhibit any light signal.

18. A data entry and display control circuit as claimed in claim 7, wherein said microprocessor is further operative in response to said second appearance of said switch signal to provide a fifth sensible control signal, said second sensible indicating means being operative in response to said fifth sensible control signal to provide a fifth sensible signal.

19. A data entry and display control circuit as claimed in claim 18, wherein said second sensible indicating means comprises audible signaling means operative in response to said fifth sensible control signal to provide a second audible signal.

20. A data entry and display control circuit as claimed in claim 19, wherein said audible signaling means comprises an audible transducer operative in response to said fifth sensible control signal to turn on and provide a tone of predetermined duration.

21. A telephone feature assignment circuit as claimed in claim 1, wherein said storage means comprises a memory.

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